WHAT IS CLAIMED IS:

1. An apparatus for storing packets comprising:

a memory for holding packets; and

a mechanism for storing at least one packet in the memory with only one packet boundary indicator associated with it.

2. An apparatus as described in Claim 1 wherein the storing mechanism includes a memory controller.

3. An apparatus as described in Claim 2 wherein the memory controller places a packet boundary indicator in the memory after a predetermined number of bits have been stored in the memory.

4. An apparatus as described in Claim 3 wherein the memory is defined by cache lines and the packets are stored along cache lines in the memory.

5. An apparatus as described in Claim 4 wherein the memory controller stores bits of data of packets in a cache line in the memory, and an identifier in the cache line of data indicating how many bits in the cache line are valid.

6. An apparatus as described in Claim 5 wherein each cache line is 200 bits long.

7. An apparatus as described in Claim 6 wherein the identifier is 2 bits of the 200 bits of each cache line.

Cont A1

8. An apparatus as described in Claim 7 wherein the memory controller inserts a packet boundary indicator after 15 cache lines worth of packets have been stored in the memory.

9. An apparatus as described in Claim 8 wherein the memory controller switches which packets are to be transferred from the memory based on packet boundary indicators with respect to priority of the packets.

10. A method for storing packets comprising the steps of:

receiving packets at a memory; and

storing with a memory controller at least one packet in the memory with only one packet boundary indicator associated with it.

11. A method as described in Claim 10 wherein the storing step includes the step of placing with the memory controller a packet boundary indicator in the memory after a predetermined number of bits have been stored in the memory.

12. A method as described in Claim 11 wherein the storing step includes the step of storing the packets along cache lines in the memory.

13. A method as described in Claim 12 wherein the placing step includes the step of storing bits of data of packets in a cache line in the memory, and an identifier in the cache line of data indicating how many bits in the cache line are valid.

Cont A1

14. A method as described in Claim 13 including after the storing step, there is the step of switching packets from the memory based on packet boundary indicators with respect to priority of the packets.